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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

| EXAMINER |
|---|
| BROCK II, PAUL E |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 04/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/609,813 | FORBES ET AL. | |
| | Examiner | Art Unit | |
| | Paul E Brock II | 2815 | |

*-- The MAILING DATE of this communication app ars on th cover sheet with the corr spond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *48-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *24* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the connecting the at least one polysilicon gate to a voltage source for producing latch-up in the multi-region planar thyristor and to a write row address line of a memory integrated circuit, and forming a plurality of channels disposed between the thyristor structures must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Specification*

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is no antecedent basis in the specification for the claim terminology of "connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit" or "forming a plurality of channels disposed between said thyristor structures".

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

*4.* Claims 62 – 65 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With regard to claim 62, it is not clear where in the originally filed specification support for connecting the at least one polysilicon gate to more than one connection can be found. For example the claim terminology "connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor and to a write row address line of a memory integrated circuit" suggests two connections to the at least one polysilicon gate. No support for a limitation of two connections to the at least one gate can be found in the originally filed specification.

With regard to claim 63, it is not clear where in the originally filed specification support for "forming a plurality of channels disposed between said thyristor structures" can be found.

With regard to claims 64 and 65, referring to the above rejection of claim 62, it is not clear where in the originally filed specification support for "connecting said at least one polysilicon gate to a voltage source" and "coupling said at least one polysilicon gate to a write row address line" can be found in the originally filed specification.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 48 – 62, 64, and 65 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 48 and 55, "incorporating said multi-region thyristor in a memory device" is a an intended use limitation. It is not clear how this intended use recitation further defines the claimed invention with respect to the method of making. Therefore, "incorporating said multi-region thyristor in a memory device," does not further distinguish the claimed invention over the prior art.

Further claim 55 recites the limitation "for producing latch-up in said multi-region planar thyristor" is an intended use recitation which does not further define the method of making the semiconductor device.

In claim 62 the phrase "for producing latchup in said multi-region planar thyristor... whereby said thyristor being adapted to transition from a first one to a second one of said at least two possible current states," is a method of using and intended use limitation. It is not clear how this method of using recitation further defines the claimed invention with respect to the method of making. Therefore, "for producing latchup in said multi-region planar thyristor... whereby said thyristor is adapted to transition from a first one to a second one of said at least two possible current states," does not further distinguish the claimed invention over the prior art.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 48 – 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueno (USPAT 5346838, Ueno) in view of Bhagat (USPAT 4861731).

Ueno discloses in figure 3 a method of forming a circuit for storing information as one of at least two possible stable current states in figures 3 – 6.

With regard to claim 48 and 55, Ueno discloses in figure 3 providing a semiconductor substrate (11). Ueno discloses in figure 3 providing doped silicon regions to from a multi-region planar thyristor having at least four regions. Ueno discloses in figure 3 forming at least one polysilicon gate (20) overlying a junction of the multi-region planar thyristor thereby making the junction a gated diode. Ueno doe not disclose that the junction is defined only by a single junction. Bhagat teaches in figure 1 forming at least one gate (54) overlying a single junction (the junction between regions 36 and 45). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the gate overlying a single junction of Bhagat in the method of Ueno in order to turn the thyristor off as stated by Bhagat in column 6, lines 15 – 18. Ueno discloses in figures 3 and 4 the gate adapted (G) to receive a voltage for producing latch-up in the multi-region planar thyristor. Ueno discloses in figures 3 and 4 incorporating said multi-region planar thyristor in a memory device.

With regard to claim 49 and 56, Ueno discloses in figure 3 providing doped silicon regions that form a seven region planar thyristor.

With regard to claim 50 and 57, Ueno discloses in figure 3 providing doped silicon regions that form a p-n-p-n-p-n-p planar thyristor.

With regard to claim 52 and 59, Ueno discloses in figure 4 the step of providing doped silicon regions further comprises forming two memory cells (CH0 and CH1)

With regard to claim 53 and 60, Ueno discloses in figures 3 and 4 connecting a central region of the seven-region planar thyristor to a shared row address line (C).

With regard to claim 54 and 61, Ueno discloses in figure 4 the step of providing doped silicon regions further comprises forming one memory cell (CH0).

With regard to claims 51 and 58, Ueno discloses a p-n-p-n-p-n-p planar thyristor. Ueno and Bhagat do not disclose an n-p-n-p-n-p-n planar thyristor. It is well known in the art to form semiconductor devices of reverse polarity. It would have been obvious to one of ordinary skill in the art at the time of the present invention to form an n-p-n-p-n-p-n planar thyristor in the method of Ueno and Bhagat for design choice of the manufacturer.

With regard to claim 62, Ueno discloses in figure 3 providing a semiconductor substrate (11). Ueno discloses in figure 3 providing doped silicon regions to from a multi-region planar thyristor having at least four regions. Ueno discloses in figure 3 forming at least one polysilicon gate (20) overlying a junction of the multi-region planar thyristor thereby making the junction a gated diode. Ueno doe not disclose that the junction is defined only by a single junction. Bhagat teaches in figure 1 forming at least one gate (54) overlying a single junction (the junction between regions 36 and 45). It would have been obvious to one of ordinary skill in the art at the

time of the present invention to use the gate overlying a single junction of Bhagat in the method of Ueno in order to turn the thyristor off as stated by Bhagat in column 6, lines 15 – 18. Ueno discloses in figures 3 and 4 connecting the at least one polysilicon gate to a voltage source (G) for producing latch-up in the multi-region planar thyristor and to write row address line of a memory integrated circuit, the thyristor being adapted to transition from a first one to a second one of the at least two possible current states. Ueno discloses in figures 3 and 4 incorporating said multi-region planar thyristor in a memory device.

With regard to claim 63, Ueno discloses in figures 3 and 6a forming a plurality of thyristor structures over a substrate (11). Ueno discloses in figures 3 and 6a forming a plurality of gates (20) disposed over respective junctions of the plurality of thyristor structures. Ueno doe not disclose that the respective junctions are defined only by respective single junctions. Bhagat teaches in figure 1 forming a plurality of gates (54) disposed over respective single junctions (the single junctions between regions 36 and 45) of the plurality of thyristor structures. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the gates disposed over respective single junctions of Bhagat in the method of Ueno in order to turn the thyristor off as stated by Bhagat in column 6, lines 15 – 18. As far as the examiner can ascertain Ueno discloses in figures 3 and 6a forming a plurality of channels disposed between the thyristor structures, whereby the thyristor structures are disposed in spaced relation to one another. Ueno discloses in figures 3, 4, and 6a mutually coupling at least two gates of the plurality of gates to a write row address line of the memory integrated circuit.

With regard to claims 64 and 65, as far as the examiner can ascertain Ueno discloses in figures 3 and 4 wherein the incorporating said multi-region planar thyristor in a memory device comprises coupling the at least one polysilicon gate to a write address line of the memory device.

***Response to Arguments***

9. Applicant's arguments filed February 26, 2003 have been fully considered but they are not persuasive.

10. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

11. With regard to the applicant's argument that "'... for producing latchup in said multi-region planar thyristor... whereby said thyristor being adapted to transition from a first one to a second one of said at least two possible current states...' This is a positive recitation of a step of a method of forming a circuit for storing information as one of at least two possible current states," it should be noted that the latch up and storing as one of at least two possible current states only occurs during intended use of the device. A method of forming a device, and the way the device is intended to be used, are two separate matters. The claims at issue define method of forming limitations. It is not clear how the intended use limitations in these method of forming

claims further distinguish the claims over the prior art. Therefore, the arguments are not persuasive, and the rejection is proper.

12. With regard to the applicant's arguments that "The further phrase 'incorporating said multi-region planar thyristor in a memory device,' is a positive recitation of a step of a method of forming a circuit or device for storing information," it should be noted that the thyristor of the present claims is disclosed as the memory device. Since the thyristor is the memory device, the step of "incorporating" the thyristor "in a memory device" can only be interpreted that the thyristor is intended to be used as a memory device. Thus, the limitation of "incorporating said multi-region planar thyristor in a memory device," is an intended use recitation. Intended use recitations do not distinguish the claimed method over the prior art. Therefore, the arguments are not persuasive, and the rejection is proper.

***Conclusion***

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 28, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800